L Number	Hits	Search Text	DB	Time stamp
-	44	processor near2 pld	USPAT	2004/08/30 13:58
-	2	6446242.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/30 11:03
-	239	(processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) near4 (non$1volatile memory) near4 (PLD$1 PAL$1 FPLA$1 CPLD$1 EPLD$1 EEPLD$1 LCA$1 FPGA$1)	USPAT	2004/08/30 14:56
-	6	5.ab.	USPAT	2004/08/30 14:02
-	6	5.clm.	USPAT	2004/08/30 14:09
-	74	(processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) near4 (non$1volatile memory) near4 (PLD$1 CPLD$1 EPLD$1 EEPLD$1)	USPAT	2004/08/30 14:20
-	56	((processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) near4 (non$1volatile memory) near4 (PLD$1 CPLD$1 EPLD$1 EEPLD$1)) same program$5	USPAT	2004/08/30 14:22
-	51	((processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) near4 (non$1volatile memory) near4 (PLD$1 CPLD$1 EPLD$1 EEPLD$1)) same program$4	USPAT	2004/08/30 14:49
-	1	6023570.pn.	USPAT	2004/08/30 14:24
-	4	(((processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) near4 (non$1volatile memory) near4 (PLD$1 CPLD$1 EPLD$1 EEPLD$1)) same program$4) same integrat$3	USPAT	2004/08/30 14:50
-	2	integrat$3 near4 (processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) near4 (((non$1volatile flash) near2 memory) EPROM EEPROM) near4 (PLD$1 PAL$1 FPLA$1 CPLD$1 EPLD$1 EEPLD$1 LCA$1 FPGA$1)	USPAT	2004/08/30 15:03
-	0	((processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) near4 (((non$1volatile flash) near2 memory) EPROM EEPROM) near4 (PLD$1 PAL$1 FPLA$1 CPLD$1 EPLD$1 EEPLD$1 LCA$1 FPGA$1)) same (single near2 packet)	USPAT	2004/08/30 15:02
-	0	built$1in near4 (processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) near4 (((non$1volatile flash) near2 memory) EPROM EEPROM) near4 (PLD$1 PAL$1 FPLA$1 CPLD$1 EPLD$1 EEPLD$1 LCA$1 FPGA$1)	USPAT	2004/08/30 15:03
-	42	(processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) near4 (((non$1volatile flash) near2 memory) EPROM EEPROM) near4 (PLD$1 PAL$1 FPLA$1 CPLD$1 EPLD$1 EEPLD$1 LCA$1 FPGA$1)	USPAT	2004/09/01 17:20
-	1	6538468.pn.	USPAT	2004/08/30 15:17

-	1	6452417.pn.	USPAT	2004/08/30 15:18
-	1	6690224.pn.	USPAT	2004/08/30 15:18
-	1	((integrat$3 adj circuit) "IC") near6 (processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) near4 (((non$1volatile flash) near2 memory) EPROM EEPROM) near4 (PLD$1 PAL$1 FPLA$1 CPLD$1 EPLD$1 EEPLD$1 LCA$1 FPGA$1)	USPAT	2004/09/01 17:23
-	227	((integrat$3 adj circuit) "IC") same (processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) same (((non$1volatile flash) near2 memory) EPROM EEPROM) same (PLD$1 PAL$1 FPLA$1 CPLD$1 EPLD$1 EEPLD$1 LCA$1 FPGA$1)	USPAT	2004/09/01 17:24
-	1	3.ab.	USPAT	2004/09/01 17:24
-	1	3.clm.	USPAT	2004/09/01 17:26
-	20	(((integrat$3 adj circuit) "IC") same (processor micro$1processor micro$1controller dsp (digital near2 signal near2 processor)) same (((non$1volatile flash) near2 memory) EPROM EEPROM) same (PLD$1 PAL$1 FPLA$1 CPLD$1 EPLD$1 EEPLD$1 LCA$1 FPGA$1)) and 710/$.ccls.	USPAT	2004/09/01 17:26